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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/092,051	03/04/2002	Stephen M. Douglass	X-923 US	7802

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XILINX, INC
ATTN: LEGAL DEPARTMENT
2100 LOGIC DR
SAN JOSE, CA 95124

EXAMINER
WHITMORE, STACY

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 07/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/092,051	DOUGLASS, STEPHEN M.	
	Examiner	Art Unit	
	Stacy A Whitmore	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *7&12/02* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claim 8 is objected to because of the following informalities:

I. As for claim 8, the phrase "that interface" is duplicated.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 4-8, 11-15, 18-19, 21, 23, 26-28, and 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Squires (US Patent 6,510,548).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

3. As for claims 1, 8, 15, and 23, Squires disclosed, the invention as claimed, including a method for designing an integrated circuit, the method comprising:

determining/identifying logic requirements - I/O requirements for an intended set of applications for the integrated circuit [col. 1, lines 13-15 where the PLD is user programmed which would include determining logic requirements for an intended set of applications, the I/O requirements would also be identified because the logic could not operate without the proper I/O requirements being identified];

determining at least one common logic function for the intended set of applications for the integrated circuit [col. 1, and especially col. 1, lines 13-15, and 49-55, where the PLD is user programmed which would include determining at least one common logic function for the intended set of logic requirements for an intended set of applications];

identifying an approximate number of configurable logic blocks and at least one fixed logic (I/O) circuit that, when combined to operate cooperatively, meet a substantial portion of the logic requirements for the intended set of applications for the integrated circuit)[col. 1, especially lines 53-56] (claim 23 - selecting a fixed logic circuit operable to meet the common logic function – fig. 5, element 501 is selected, and the I/O circuitry is also identified);

designing the integrated circuit to include the approximate number of configurable logic blocks formed as a fabric and arranged to (at least partially) surround an opening in the fabric [col. 1, and fig. 5, element 501 is surrounded by CLB's];

designing the integrated circuit to include the at least one fixed logic circuit in the opening in the fabric [col. 1, "the core is included in the opening in the fabric, see fig. 5, element 501, which is provided in an opening in the fabric of CLB's]; and

designing the integrated circuit to include interconnecting logic that interfaces the at least one fixed logic circuit to the fabric [col. 1, and fig. 5, elements 501a – 501c].

(claim 23) designing the IC to include the approximate number of CLBs, the fixed logic circuit, and the fixed logic I/O circuit [col. 1, and fig. 5].

4. As for claims 4-5, 11-12, 19, and 27, Squires disclosed wherein the at least one fixed logic circuit is selected from the group consisting of digital signal processors, microprocessors, physical layer interfaces, link layer interfaces, network layer interfaces, audio processors, video graphics processors, and applications specific integrated circuits [col. 1, especially dsp]; and

wherein the intended applications include at least one of communications applications, system-on-a-chip applications, image processing applications, parallel processing applications, networking applications, serial processing applications, and prototyping applications [col. 1, dsp functions include communications applications, image processing, parallel and serial applications].

5. As for claims 6-7, 13-14, 21, 28 and 30, Squires disclosed wherein the logic requirements are characterized by parameters including at least one of data processing requirements, data storage requirements, data throughput requirements, instruction set type, and instruction set contents [col. 1, lines 13-15 where the PLD is user programmed which would include data processing requirements, data storage requirements, and data throughput requirements because the designed logic could not operate without the proper data requirements being characterized]; and
wherein the integrated circuit occupies a die area [col. 1]; and the fixed logic circuit occupies less than a predetermined percentage of the die area [fig. 5, element 501, reads on the less than a predetermined area because the area held for the logic is predetermined].

6. As for claims 18 and 26, Squires disclosed at least one fixed logic input/output circuit is selected from the group consisting of high speed serial input/output circuits and high speed parallel input/output circuits [col. 2, lines 23-27, the term high speed is a relative term which is not limited in scope to a certain rate and therefore any serial or parallel I/O reads on the limitation].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2-3, 9-10, 16-17, 20, 24-25, 29, and 32 are rejected under 35 U.S.C. 103(a) as being obvious over Squires (US Patent 6,510,548) in view of Ting (US Patent 5,457,410).

The applied reference Squires '548 has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). For applications filed on or after November 29, 1999, this rejection might also be overcome by showing that the subject matter of the reference and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person. See MPEP § 706.02(l)(1) and § 706.02(l)(2).

8. As for claims 2-3, 9-10, 16,17, 20, 24-25, 29, and 32, Squires disclosed the invention substantially as claimed, including the method of designing an integrated circuit as cited in the rejections of claims 1, 8, 15, and 23 above.

Squires did not specifically disclose

selecting a die size for the integrated circuit; and

designing the integrated circuit such that the configurable logic blocks and the at least one fixed logic circuit it within a targeted die size.

selecting a process for manufacturing of the integrated circuit, wherein the process involves a minimum dimension size for the integrated circuit; and selecting a die size for the integrated circuit considering the process, the approximate number of configurable logic blocks of the at least one fixed logic circuit.

[claims 20 and 29] wherein the input/output requirements are characterized by parameters including at least one of bit rate input, bit rate output, data width, address width, parallel bus frequency.

Ting disclosed selecting a die size for the integrated circuit; and designing the integrated circuit such that the configurable logic blocks and the at least one fixed logic circuit it within a targeted die size; and selecting a process for manufacturing of the integrated circuit, wherein the process involves a minimum dimension size for the integrated circuit; and selecting a die size for the integrated circuit considering the process, the approximate number of configurable logic blocks of the at least one fixed logic circuit [col. 3, lines 45-60].

[claims 20 and 29] wherein the input/output requirements are characterized by parameters including at least one of bit rate input, bit rate output, data width, address width, parallel bus frequency [col. 6, lines 16-17].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Squires and Ting because Squires disclosed a method of designing a circuit with configurable and fixed logic on a circuit die as cited in the rejections of claims 1, 8, 15, and 23. Ting also disclosed the design of configurable and fixed logic on a circuit die with the optimization of circuit die area with the consideration of the circuit area used by the logic. Adding Ting's optimization of targeted circuit area on the die would have improved Squires method by providing a parameter for design that would optimize die size and therefore result in a circuit design that would reduce the cost of producing the integrated circuit. Further, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Squires and Ting because adding Ting's I/O requirements of data width would have enabled Squires to design circuit routing (bit and word lines) with a minimum of space thereby utilizing parameters for designing an integrated circuit that is optimized for area constraints of the die size.

9. As for claim 32, Squire disclosed the invention substantially as claimed, including the method of circuit design as disclosed above in the rejections of claims 1, 8, 15, and 23.

Squires did not specifically disclose wherein the fixed logic input/output circuit and the fixed logic processing circuit access common block ram segments

Ting further disclosed wherein the fixed logic input/output circuit and the fixed logic processing circuit access common block ram segments [col. 2, lines 57-60].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Squires and Ting because adding Ting's common block ram segments would have improved Squires method by having user

defined logic that is accessible within the CLBs thereby providing for a reduced circuit size improving design efficiency.

10. Claims 22 and 31 are rejected under 35 U.S.C. 103(a) as being obvious over Squires (US Patent 6,510,548) in view of Andrew, W.B., "A field programmable system chip which combines FPGA and ASIC circuitry".

The applied reference Squires '548 has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). For applications filed on or after November 29, 1999, this rejection might also be overcome by showing that the subject matter of the reference and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person. See MPEP § 706.02(l)(1) and § 706.02(l)(2).

11. As for claims 22 and 31, Squires disclosed the method of designing an integrated circuit as cited above in the rejections of claims 1, 8, 15, and 23.

Squires did not specifically disclose wherein the at least one fixed logic input/output circuit resides at an edge of the fabric.

Andrew disclosed wherein the at least one fixed logic input/output circuit resides at an edge of the fabric [pg. 183, fig. 1].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Squires and Andrew because adding Andrew's at least one fixed logic input/output circuit resides at an edge of the fabric would have improved Squires method by providing easy access to from the fixed logic to the external circuit for easy programming or I/O the external peripherals which could reduce area required by the circuit design.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A Whitmore whose telephone number is (703) 305-0565. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (703) 308-3325. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7724 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Stacy A Whitmore
Patent Examiner
Art Unit 2812

SAW
July 16, 2003